Mass-parallel Sleptsov Net-Based Solving PDEs on FPGA for Embedded Control

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Embedded System Design

- Target device:
 - Microcontrollers (MCs)
 - Field-Programmable Gate Array (FPGA)
- Design approach (bare hardware, RTOS):
 - Direct coding
 - Model-driven development (UML)
 - Formal (math) method driven development

Workflow



Laplace Equation Case Study

 $\frac{\partial^2 u(x,y)}{\partial x^2} + \frac{\partial^2 u(x,y)}{\partial y^2} = 0$



Stencil with accuracy O(h⁴)

$$\frac{\partial^2 u_{i,j}}{\partial y^2} = \frac{u_{i+1,j+1} - 2u_{i+1,j} + u_{i+1,j-1} + u_{i,j+1} - 2u_{i,j} + u_{i,j-1} + u_{i-1,j+1} - 2u_{i,j-1} + u_{i-1,j-1}}{3h^2}$$
Finite difference approximation of derivative

Laplace

equation

$$u_{i,j}^{(s+1)} = \frac{4\left(u_{i,j-1}^{(s)} + u_{i-1,j}^{(s)} + u_{i,j+1}^{(s)} + u_{i+1,j}^{(s)}\right) + u_{i-1,j-1}^{(s)} + u_{i+1,j+1}^{(s)} + u_{i-1,j-1}^{(s)} + u_{i+1,j-1}^{(s)}}{20}$$

Finite difference expression

Termination Condition and Example

Termination condition

$$\max_{i,j} \left| u_{i,j}^{(s+1)} - u_{i,j}^{(s)} \right| < \varepsilon$$

Constant boundary Numerical example

$$u(x, 0) = 1, 0 \le x \le 1$$

$$u(0, y) = 0, 0 < y \le 1$$

$$u(x, 1) = 0, 0 \le x < 1$$

$$u(1, y) = 1, 0 \le y \le 1$$



Sleptsov Net Computing

- https://dimazaitsev.github.io/snc.html
- Bipartite directed graph
- Vertices: places and transitions
- Tokens inside places net marking
- Weigh (multiplicity) of arcs
- Marking changes as a result of transition firing
- Turing-complete system

Transition Firing Rule



 $C(p,t) = \mu(p)/A(p,t)$ Firing multiplicity of arc

 $C(t) = \min_{A(p,t)>0} C(p,t)$ Firing multiplicity of transition

$$\mu(p)^{k+1} = \mu(p)^{k} - \sum_{A(p,t)>0} C(t) \cdot A(p,t) + \sum_{A(t,p)>0} C(t) \cdot A(p,t)$$
 Next marking

One node iteration SN





one time cycle per iteration

three time cycles per iteration

5x5 (3x3 non-boundary) lattice







three time cycles per iteration

Infinite Parametric SN Specification

Internal nodes

$$\begin{pmatrix} div5_{i,j}: 5 \cdot u_{i,j} \to u_{i-1,j}, u_{i-1,j}^{'}, u_{i+1,j}, u_{i+1,j}^{'}, u_{i,j-1}, u_{i,j-1}^{'}, u_{i,j+1}, u_{i,j+1}^{'}, u_{i,j+1}^{'}, u_{i,j+1}, u_{i,j+1}^{'}, u_{i+1,j-1}^{'}, u_{i+1,j-1}^{'}, u_{i+1,j+1}^{'}, u$$

 $1 \le i \le N-1, 1 \le j \le N-1$

Border nodes

$$\begin{pmatrix} div5_{i,j}: 5 \cdot u_{i,j} \to 5 \cdot u_{i,j}, u_{i-1,j}, u_{i+1,j}, u_{i,j-1}, u_{i,j+1}, \\ div20_{i,j}: 20 \cdot u_{i,j}' \to 20 \cdot u_{i,j}', u_{i-1,j-1}', u_{i-1,j+1}', u_{i+1,j-1}', u_{i+1,j+1}' \end{pmatrix}$$

$$i = 0, i = N - 1, j = 0, \qquad j = N - 1$$

Verilog Code Generated

```
always @(posedge sys clk) begin
  if (counter < `K ) begin
    for(i = 1; i < `N-1; i = i+1) begin // iterate
     for(i = 1; i < N-1; i = i+1) begin
       cross=u[i+1][j]+u[i-1][j]+u[i][j+1]+u[i][j-1];
      diag=u[i+1][j+1]+u[i+1][j-1]+
                 u[i-1][j+1]+u[i-1][j-1];
      num=4*cross+diag;
      u1[i][j] = num/20+((num%ROUND EDGE)<11)?0:1;
     end
    end
    for(i = 1; i < `N-1; i = i+1) begin // u=u1;
     for(j = 1; j < `N-1; j = j+1) begin
      u[i][i] = u1[i][i];
     end
    end
  end
  else
   led = ~ u[2][2][5:0];
  end
```

Synthesized FPGA circuit layout





Benchmarks



real numbers

integer approximation on FPGA

Dependence of the solution time (number of iterations) on the actual accuracy of approximation

For 50MHz clock, we run an iteration in about 20 ns

Conclusions

- Fast mass-parallel numerical solving of optimal control problems specified by PDE
- Embedded control of fast processes in real time on FPGA
- Formal method driven development
- Finite difference methods
- Graphical language of infinite Sleptsov nets

Recent advances

- D.A. Zaitsev, T.R. Shmeleva, A.A. Kostikov, Computing and Communication Structure Design for Fast Mass-Parallel Numerical Solving PDE, <u>Parallel</u> <u>Processing Letters, May 9, 2025.</u>
- D. A. Zaitsev, Y. Ajima, J. F. C. Bartlett, and A. Kumar, 3D multicore CPU vs GPU on sparse patterns of Sleptsov net virtual machine, <u>International Journal of</u> <u>Parallel, Emergent and Distributed Systems, 16 Apr 2025.</u>
- R. Xu, S. Zhang, D. Liu and D. A. Zaitsev, "Sleptsov net based reliable embedded system design on microcontrollers and FPGAs," <u>2024 IEEE</u> <u>International Conference on Embedded Software and Systems (ICESS),</u> <u>Wuhan, China, 2024, pp. 1-8.</u>
- B. Berthomieu, D.A. Zaitsev, Sleptsov Nets are Turing-complete, <u>Theoretical</u> <u>Computer Science, Volume 986, 2024, 114346, ISSN 0304-3975.</u>