



Task 3: Sequential logic digital circuit design in Verilog

Design a sequential circuit on a state machine using a given type of flip-flops

Individual variant: state machine examples from lectures, type of flip-flops

Subtasks:

- 1) Encode a given state machine in binary numbering system
- 2) Synthesize and minimize Boolean functions switching states and output
- 3) Compose a Verilog module to represent the state machine based on a sub-module of flip-flop
- 4) Obtain graphical layout of the sequential circuit
- 5) Implement manual testing of the circuit
- 6) Implement direct synthesis of state machine without explicit composition of Boolean function, compare obtained circuits

Optional study: automatic testing of sequential circuits in Verilog.

Directions:

- Choose idle items encoded with low energy
- For minimization of Boolean functions use Karnaugh maps for up to 4 variables and online tools for bigger number of variables
- Debug the flip-flop module first, then use it
- Try to follow the state diagram when testing, save a few images

Questions to muse:

References:

- Lecture 4 – Digital circuits design with Verilog. Sequential logic
- Lecture 3 – Digital circuits design with Verilog. Combinatorial logic
- Lecture 2 – Modeling Embedded Systems by Finite Automata (State Machines)

Supplemental materials: Overview of propositional logic

Task variants:

Student number	1-5	6-10
Task	Vending machine	Lift control in 3 storey building

Student no.	$N \bmod 3 = 0$	$N \bmod 3 = 1$	$N \bmod 3 = 2$
Flip-flop	T	RS	JK

