

WSIZ, 2023
Computer systems architecture

Lecture 12.

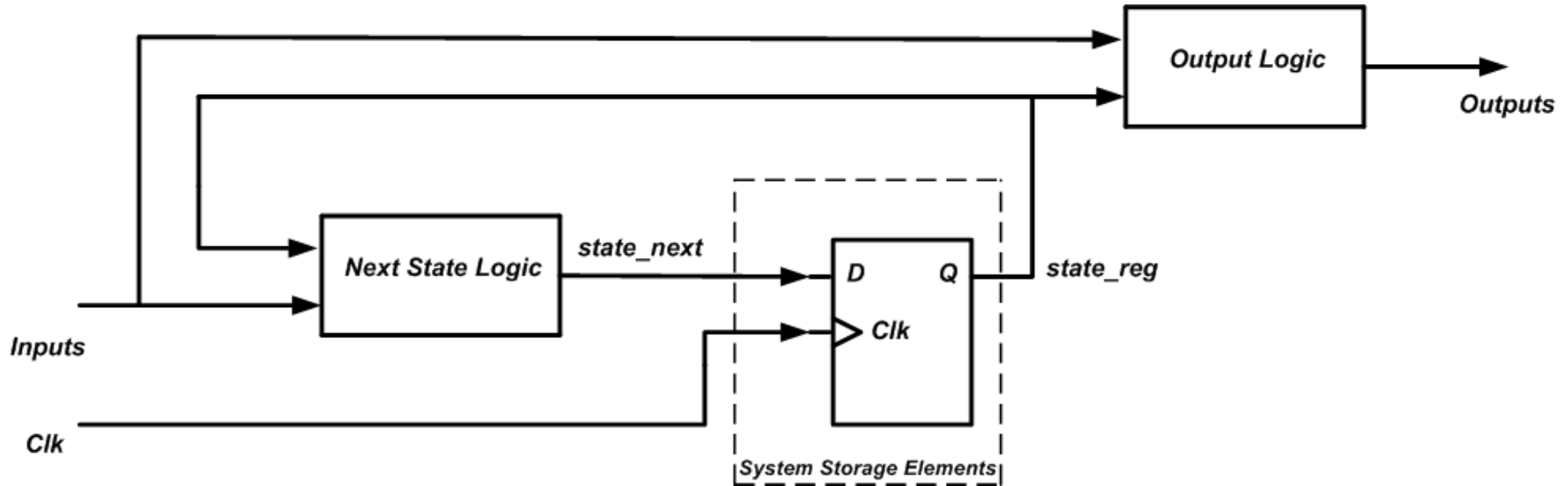
Synthesis of sequential logic circuits in

Verilog

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<http://daze.ho.ua>

Sequential logic layout



Sequential Logic in Verilog

- Define blocks that have memory: Flip-Flops, Latches, Finite State Machines
- Sequential Logic is triggered by a 'CLOCK' event: latches are sensitive to level of the signal; flip-flops are sensitive to the transitioning of clock
- New constructs: always, initial

Verilog number representation

Verilog	Stored Number	Verilog	Stored Number
4'b1001	1001	4'd5	0101
8'b1001	0000 1001	12'hFA3	1111 1001 0011
8'b0000_1001	0000 1001	8'o12	00 001 010
8'bxX0X1zZ1	XX0X 1ZZ1	4'h7	0111
'b01	0000 .. 0001	12'h0	0000 0000 0000

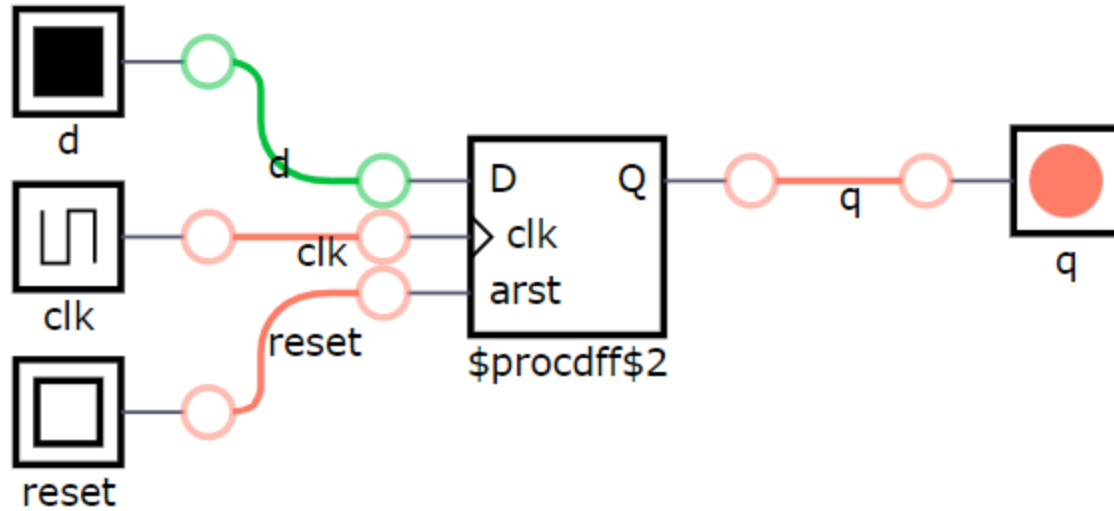
Statement Always

- **always @ (sensitivity list)
statement;**
- Whenever the event in the sensitivity list occurs, the statement is executed

Flip-flop Verilog specification

```
module D_FF (  
    input wire clk, reset,  
    input wire d,  
    output reg q);  
    always @(posedge clk, posedge reset)  
        if (reset)  
            q <= 1'b0;  
        else  
            q <= d;  
endmodule
```

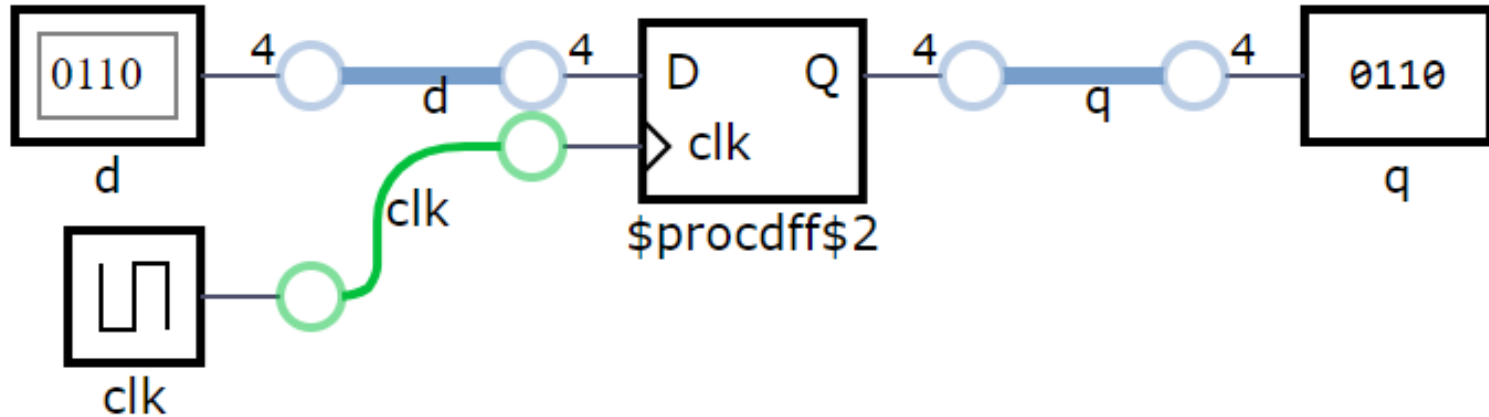
Flip-flop layout



D Flip-Flop register

```
module flop(  
    input clk,  
    input [3:0] d,  
    output reg [3:0] q);  
always @ (posedge clk)  
    q <= d;  
endmodul
```


D Flip-Flop register layout



Event Posedge

- always @ (posedge clk)
 q <= d;
- The posedge defines a rising edge (transition from 0 to 1)
- This process will trigger only if the clk signal rises

Non blocking assignment

- 'assign' statement is not used within always block
- The "<=" describes a 'non-blocking' assignment
- Assigned variables need to be declared as reg

D Flip-Flop with Asynchronous Reset

```
module flop_ar (  
    input clk,  
    input reset,  
    input [3:0] d,  
    output reg [3:0] q);  
always @ (posedge clk, negedge reset)  
begin  
    if (reset == '0') q <= 0;    // when reset  
    else q <= d;                // when clk end  
end  
module
```

D Flip-Flop with Synchronous Reset

```
module flop_sr (  
    input clk,  
    input reset,  
    input [3:0] d,  
    output reg [3:0] q);  
always @ (posedge clk)  
begin  
    if (reset == '0') q <= 0;        // when reset  
    else q <= d;                    // when clk  
end  
endmodule
```

Sequential Statements in Verilog

- Sequential statements are within an 'always' block
- The sequential block is triggered with a change in the sensitivity list
- Signals assigned within an always must be declared as reg
- We use `<=` for (non-blocking) assignments and do not use 'assign' within the always block

Bidirectional Counter (BC)

- When the “load” input is asserted, the input data (d) is loaded into the counter ($q=d$).
- When both “load” and “en” are logic low, the counter keeps its current value.
- For “load”=0 and “en”=1, the counter may count either upward or downward depending on the value of the “up_downb” input.

Formal specification of BC

Table 1

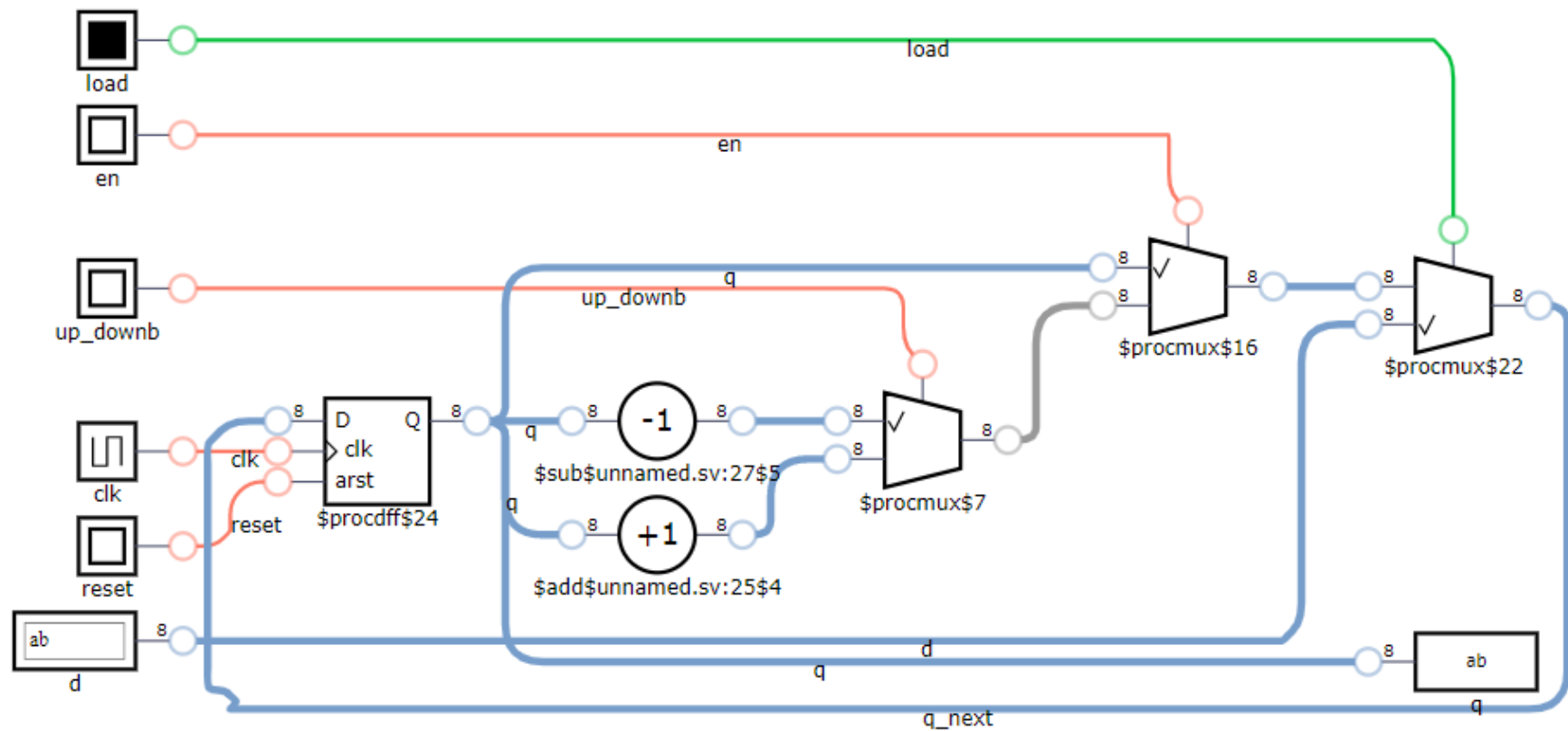
Function	load	en	up_downb	Output(q)
Load	1	x	x	d
No Operation	0	0	x	q
Count Up	0	1	1	q+1
Count Down	0	1	0	q-1

Verilog specification of BC

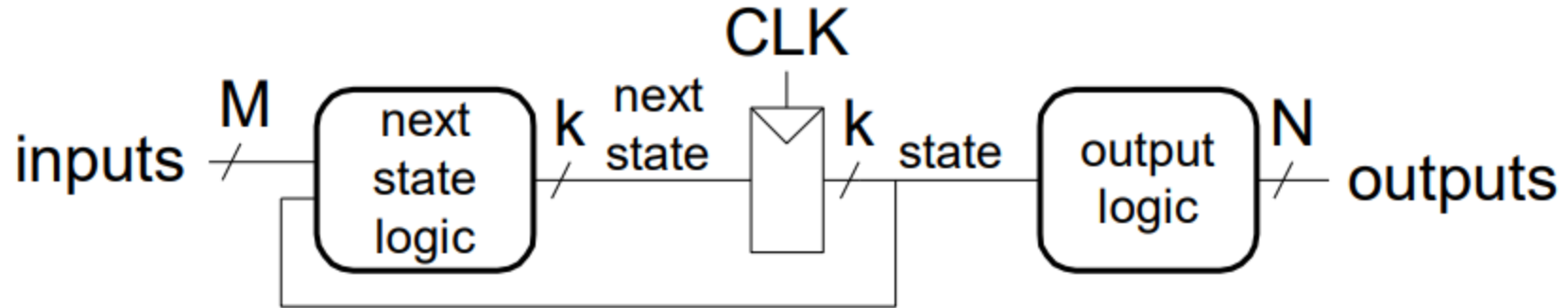
```
module bidirect_cnt8 (  
    input wire clk, reset,  
    input wire en, load, up_downb,  
    input wire [7:0] d,  
    output reg [7:0] q );  
    reg [7:0] q_next;  
    // The storage elements  
    always @(posedge clk, posedge  
reset)  
    if (reset)  
        q <= 8'h00;  
    else  
        q <= q_next;
```

```
//The next state logic  
always @*  
if(load)  
    q_next = d;  
else if (~en)  
    q_next = q;  
else if (up_downb)  
    q_next = q + 8'h01;  
else  
    q_next = q - 8'h01;  
endmodule
```

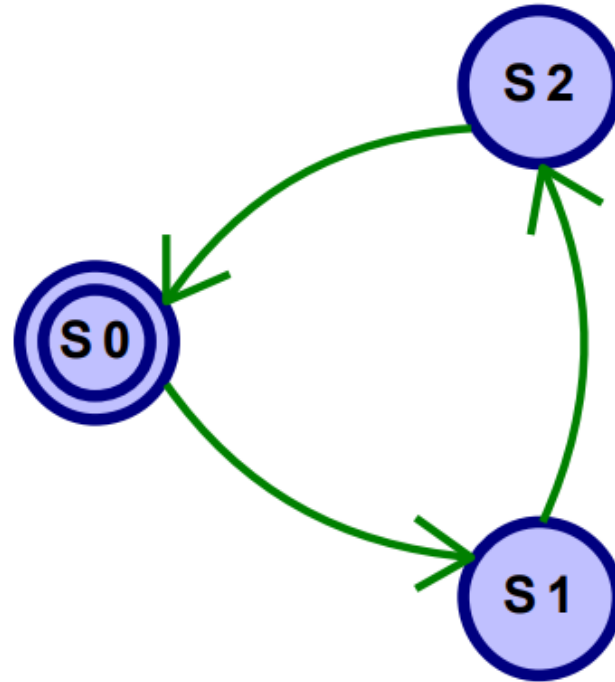
BC layout



Direct implementation of state machine in Verilog



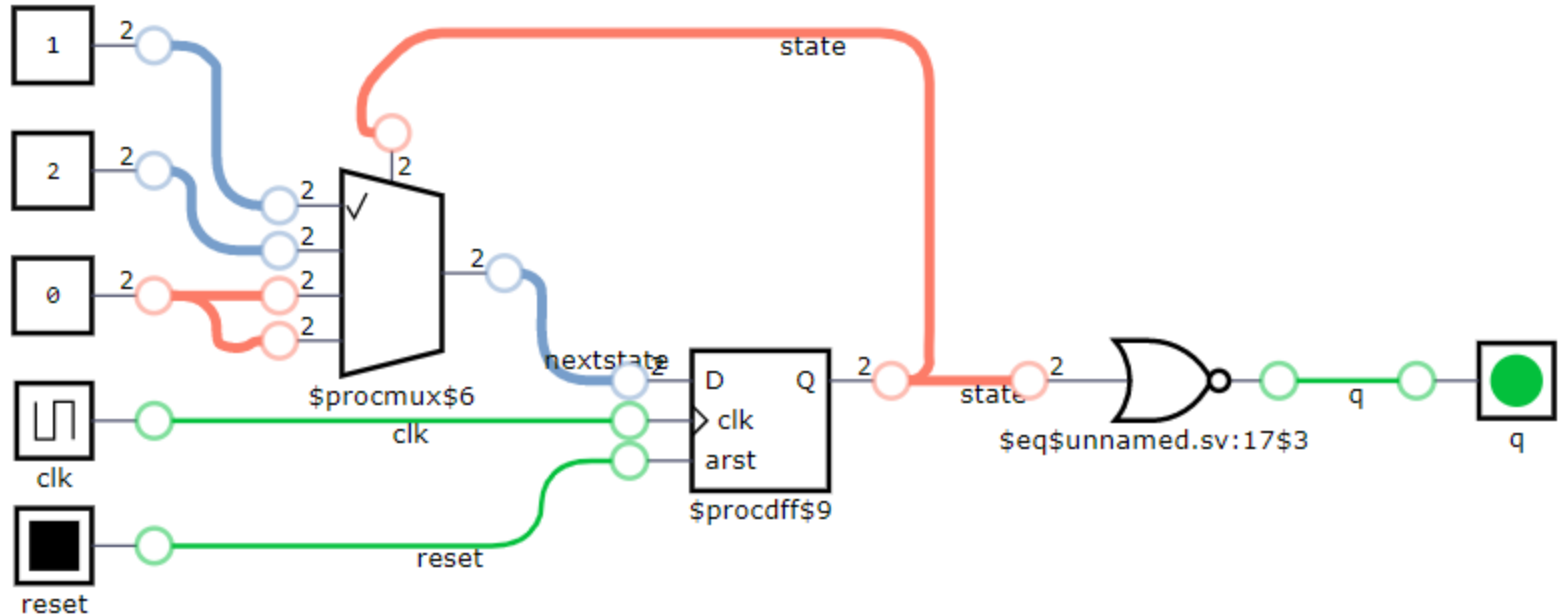
Counter module 3



Verilog code of counter module 3

```
module counter3FSM (  
    input clk,  
    input reset,  
    output q);  
    reg [1:0] state, nextstate;  
    parameter S0 = 2'b00; parameter S1 = 2'b01; parameter S2 = 2'b10;  
    always @ (posedge clk, posedge reset) // state register  
        if (reset) state <= S0;  
        else state <= nextstate;  
    always @ (*) // next state logic  
        case (state)  
            S0: nextstate = S1;  
            S1: nextstate = S2;  
            S2: nextstate = S0;  
            default: nextstate = S0;  
        endcase  
    assign q = (state == S0); // output logic  
endmodule
```

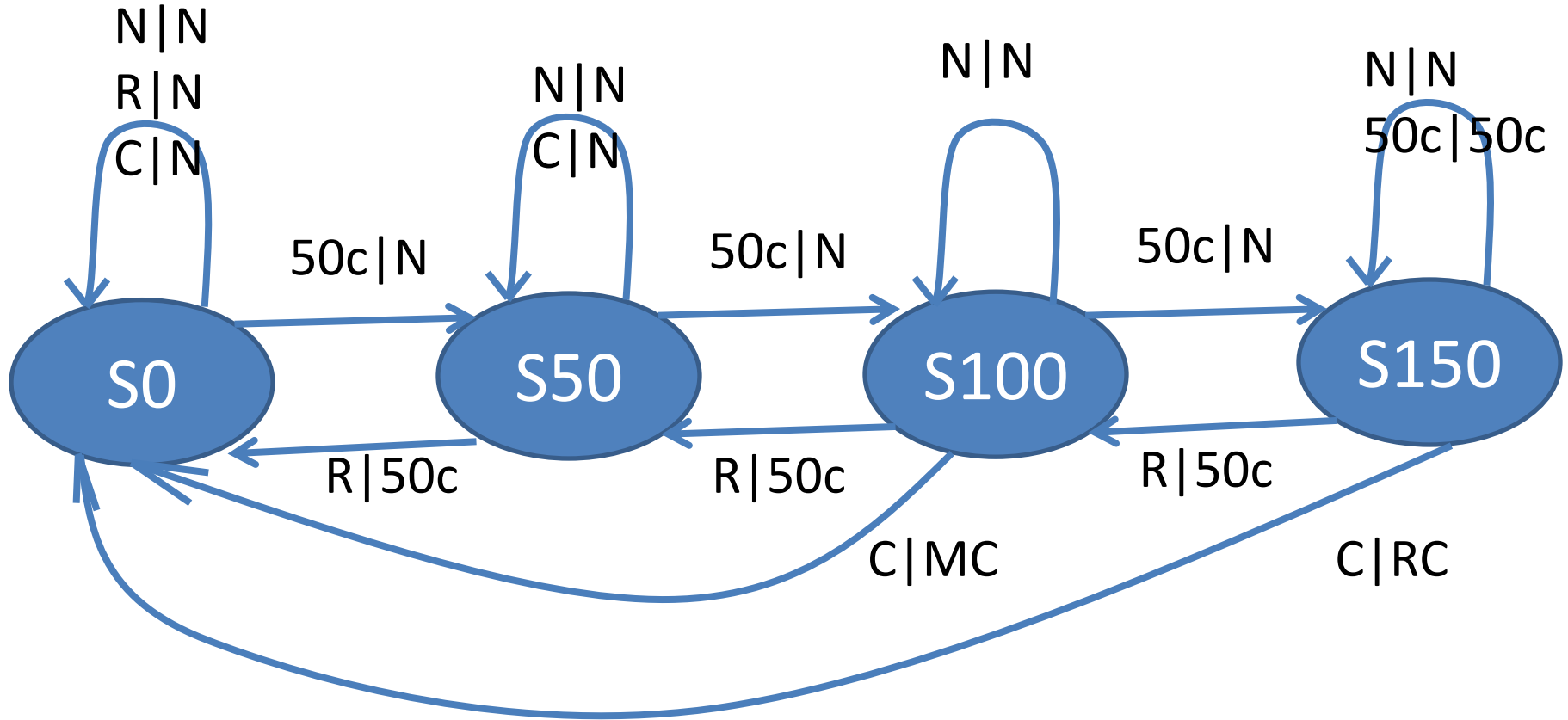
Counter module 3 layout



Chocolate vending machine

- Input: 50c, R, C, N
- Output: milk chocolate (1e), rum chocolate (1.5e), 50c, N
- State: s0, s50, s100, s150

State diagram



Binary encoding of inputs, outputs, and states

Input	Code	
	x1	x0
N	0	0
C	0	1
50c	1	0
R	1	1

Output	Code	
	y1	y0
N	0	0
MC	0	1
50c	1	0
RC	1	1

State	Code	
	q1	q0
q0	0	0
q50	0	1
q100	1	0
q150	1	1

Direct implementation

```
module chockM (  
    input clock,           // clock signal  
    input reset,           // reset signal  
    input [1:0] i,         // encoded input  
    output reg [1:0] o);   // encoded output  
    reg [1:0] state, next_state; // current and next state  
    parameter S0 = 2'b00;  // codes of states  
    parameter S50 = 2'b01;  
    parameter S100 = 2'b10;  
    parameter S150 = 2'b11;  
    parameter c50 = 2'b10; // codes of input and output symbols  
    parameter C = 2'b01;  
    parameter R = 2'b11;  
    parameter MC = 2'b01;  
    parameter RC = 2'b11;  
    parameter N = 2'b00;
```

// next state

```
always @*
begin
case(state)
S0: if (i==c50) next_state=S50;
    else next_state=S0;
S50: if (i==c50) next_state=S100;
    else if (i==R) next_state=S0;
    else next_state=S50;
S100: if (i==c50) next_state=S150;
    else if (i==R) next_state=S50;
    else if (i==C) next_state=S0;
    else next_state=S100;
S150: if (i==R) next_state=S100;
    else if (i==C) next_state=S0;
    else next_state=S150;
default: next_state=S0;
endcase
end
```

// replace state

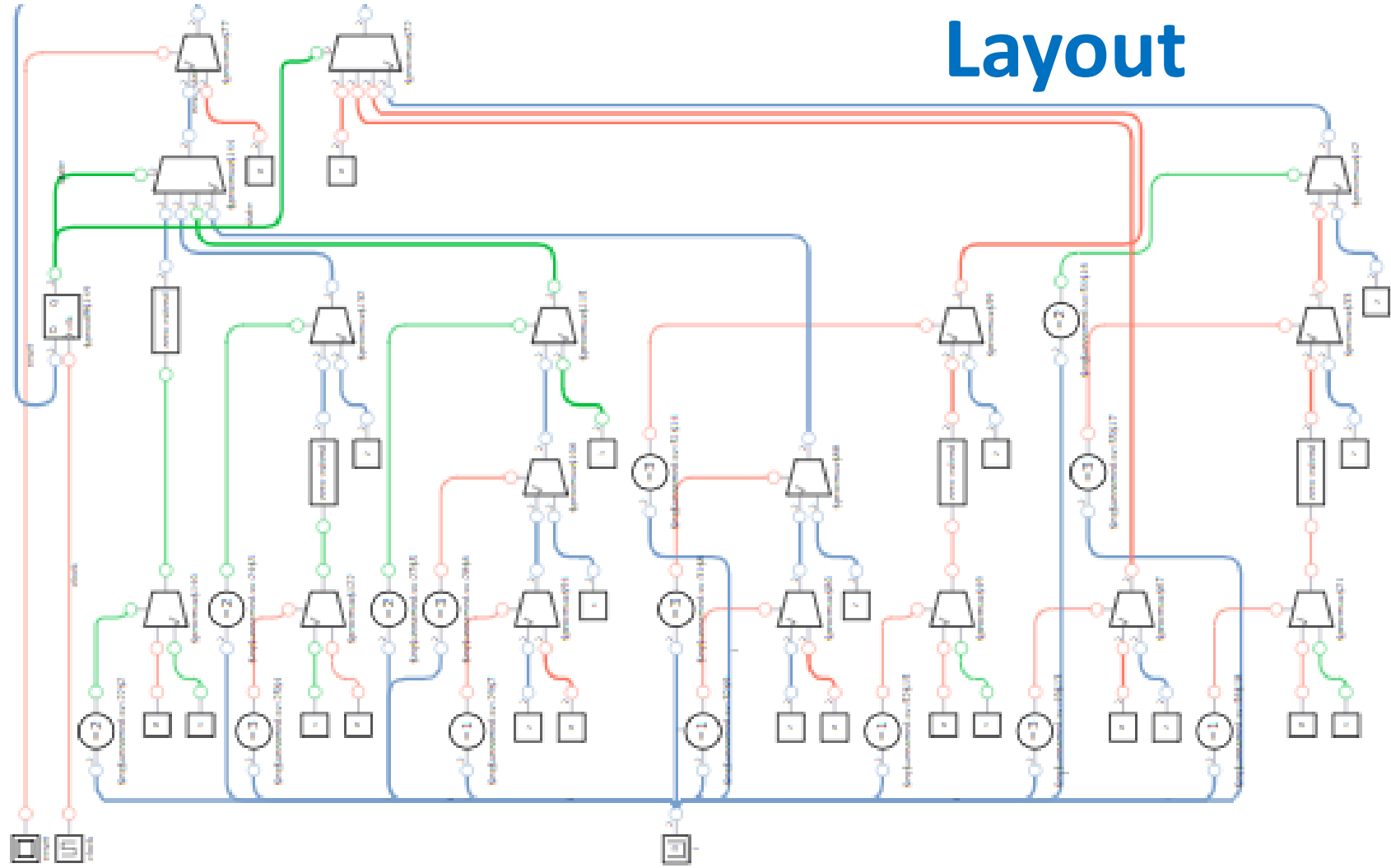
```
always @ (posedge clock)
begin
    if (reset == 1'b1)
        state <= S0;
    else
        state <= next_state;
end
```

// output signal

```
always @*
begin
case(state)
S50: if (i==R) o=c50;
    else o=N;
S100: if (i==R) o=c50;
    else if (i==C) o=MC;
    else o=N;
S150: if (i==c50) o=c50;
    else if (i==R) o=c50;
    else if (i==C) o=RC;
    else o=N;
default: o=N;
endcase
end

endmodule
```

Layout



Simulating

Microsoft Word - verilog_ref_seqv2.x | DigitalJS Online | verilog - Error "procedural assign" | graphviz - Yosys -- producing an | +

Not secure | digitaljs.tilk.eu/#b22408580b84d52d150ae5a6179ef658b3b5b56160763af3591be582454fe940

82996

reset

clock

state

\$sprocdff\$149

\$sprocmux\$140

zero-extend

\$sprocmux\$144

\$sprocmux\$77

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Truth table

q1	q0	x1	x0	q1	q0	y1	y0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	1	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	1	0	1	0

Boolean functions

	q ₁			
q\ <i>x</i>	00	01	11	10
00				
01				1
11	1		1	1
10	1			1

	q ₀			
q\ <i>x</i>	00	01	11	10
00				1
01	1	1		
11	1			1
10			1	1

$$q_1 = q_1 \bar{x}_0 \vee q_1 q_0 x_1 \vee q_0 x_1 \bar{x}_0$$

$$q_0 = \bar{q}_0 x_1 \bar{x}_0 \vee \bar{q}_1 q_0 \bar{x}_1 \vee q_1 q_0 \bar{x}_0 \vee q_1 \bar{q}_0 x_1$$

	y ₁			
q\ <i>x</i>	00	01	11	10
00				
01			1	
11		1	1	1
10			1	

	y ₀			
q\ <i>x</i>	00	01	11	10
00				
01				
11		1		
10		1		

$$y_1 = q_0 x_1 x_0 \vee q_1 q_0 x_1 \vee q_1 x_1 x_0 \vee q_1 q_0 x_0$$

$$y_0 = q_1 \bar{x}_1 x_0$$

```

module chockM (
    input clock,
    input reset,
    input [1:0] i,
    output reg [1:0] o;
    reg [1:0] state, next_state;

always @* // next state computation
begin
    next_state[1] = state[1]&~i[0] | state[1]&state[0]&i[1] | state[0]&i[1]&~i[0];
    next_state[0] = ~state[0]&i[1]&~i[0] | ~state[1]&state[0]&~i[1] | state[1]&state[0]&~i[0] |
state[1]&~state[0]&i[1];
end

always @ (posedge clock) // state switching
begin
    if (reset == 1'b1)
        state <= 2'b00;
    else
        state <= next_state;
end

always @* // Output logic-determines outputs from current state
begin
    o[1] = state[0]&i[1]&i[0] | state[1]&state[0]&i[1] | state[1]&i[1]&i[0] | state[1]&state[0]&i[0];
    o[0] = state[1]&~i[1]&i[0];
end

endmodule

```

Verilog

Layout

