

WSIZ, 2023

Computer systems architecture

Dmitry Zaitsev

<http://daze.ho.ua>

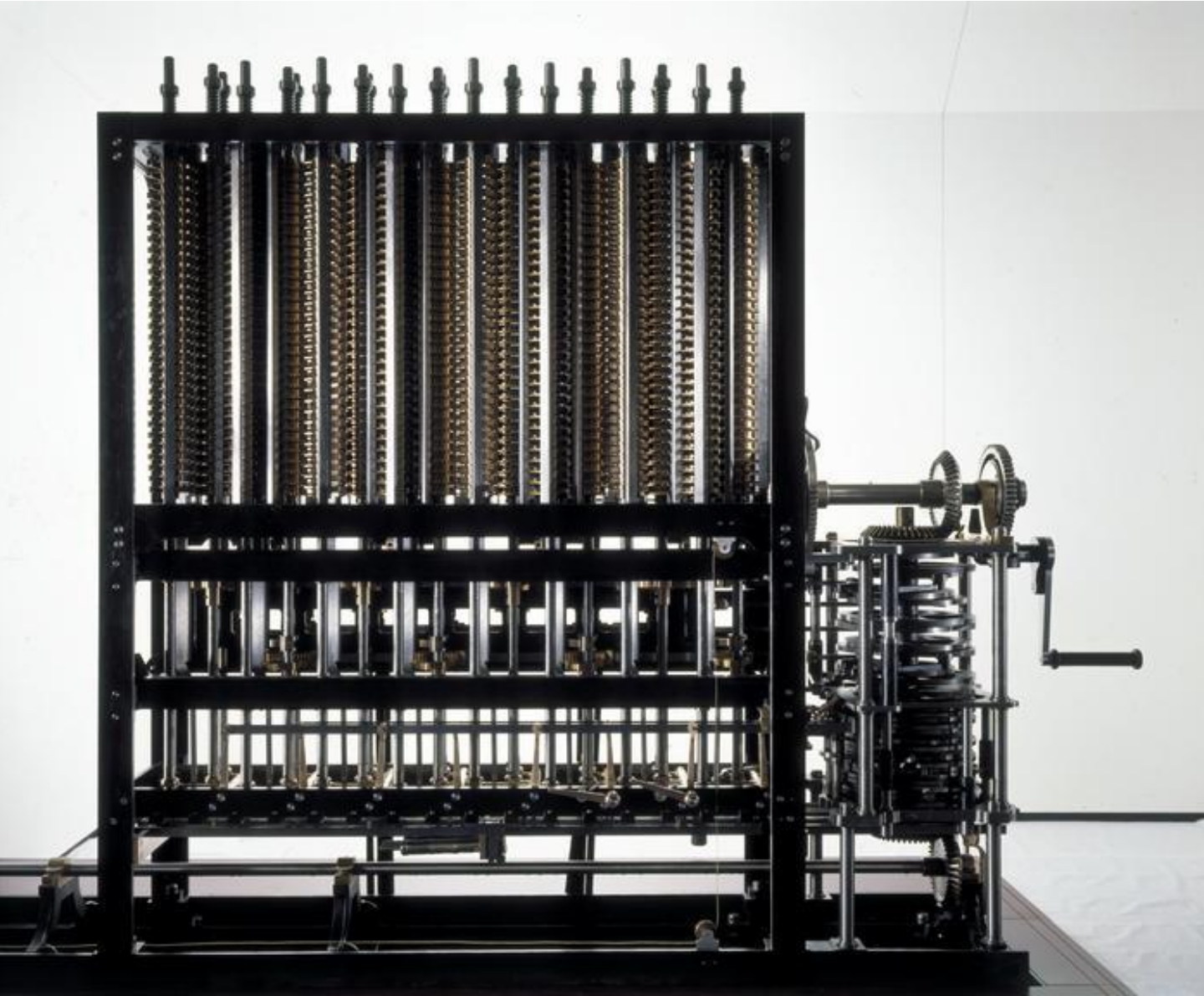
WSIZ, 2023

Lecture 1. Introduction. Von Neumann Architecture

Dmitry Zaitsev
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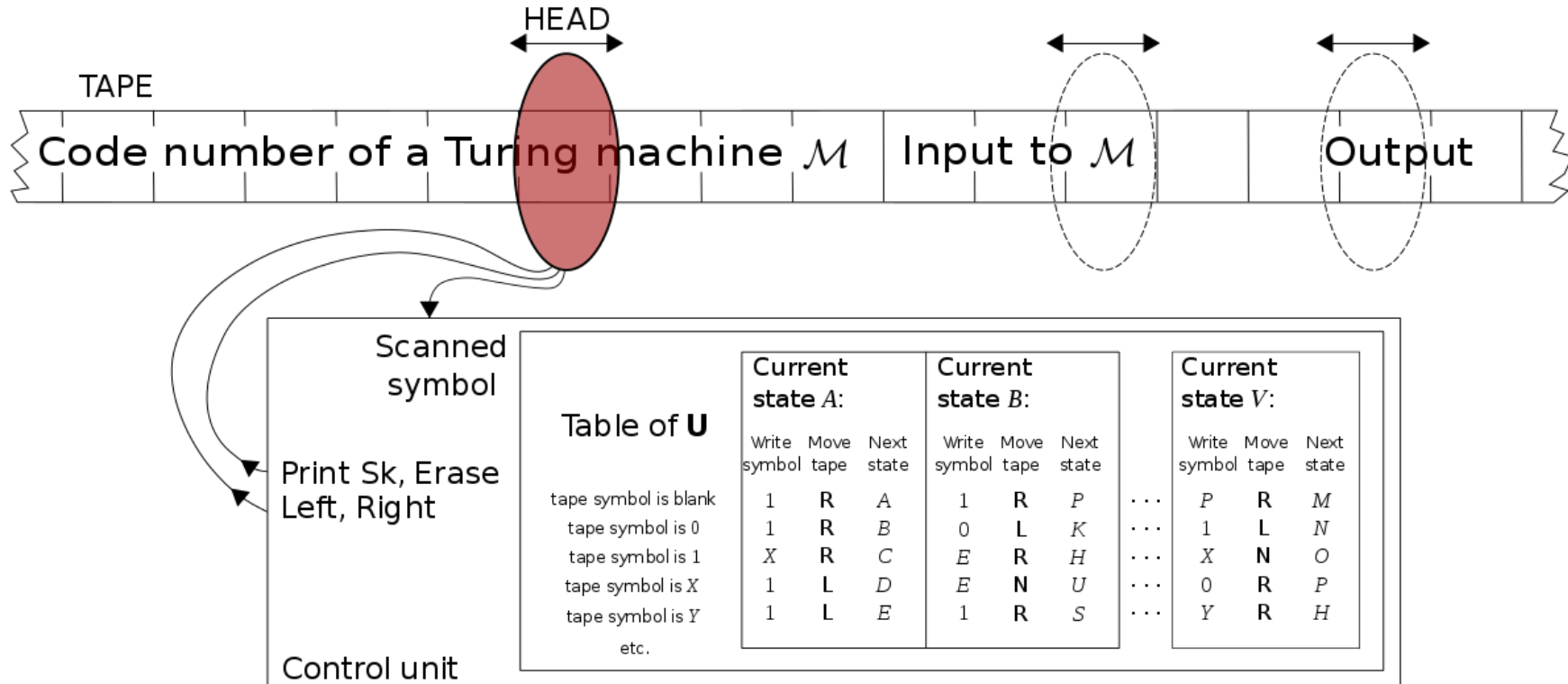
Historical prototypes of computer

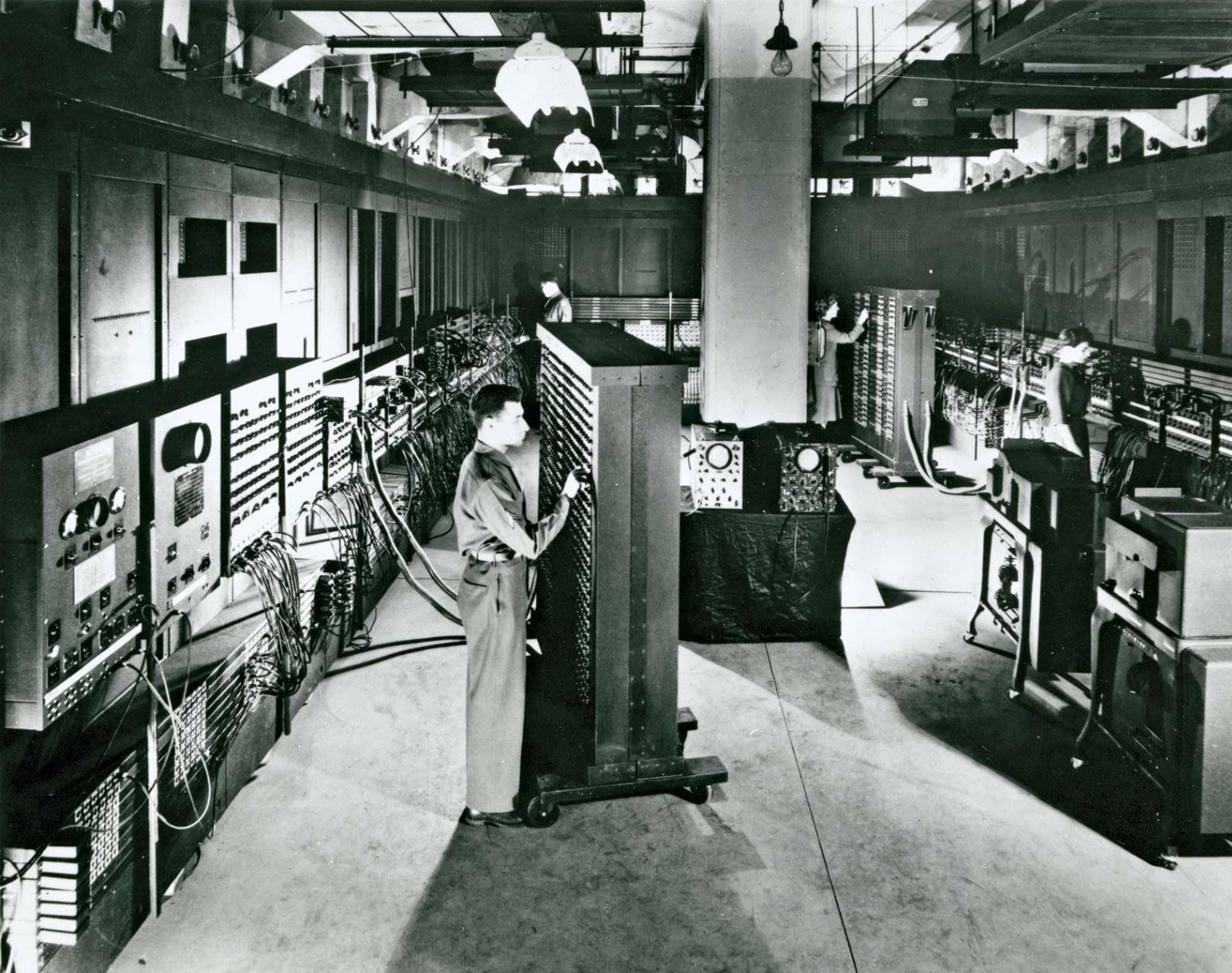
- **1821:** English mathematician Charles Babbage conceives of a steam-driven calculating machine that would be able to compute tables of numbers.
- **1848:** Ada Lovelace writes the world's first computer program for computation of Bernoulli numbers with Babbage's machine.
- **1936:** Alan Turing presents the principle of a universal machine
- **1945:** Two professors at the University of Pennsylvania, John Mauchly and J. Presper Eckert, design and build the Electronic Numerical Integrator and Calculator (ENIAC).
- **1948:** MESM (Small Electronic Calculating Machine), Kyiv was the first universally programmable electronic computer in continental Europe



**Difference
Engine No 2,
designed by
Charles
Babbage**

Universal Turing Machine





ENIAC



MESM

Generations of computers

- First Generation Computers: Vacuum Tubes (1940-1956): IBM 650, IBM 701, ENIAC, UNIVAC1
- Second Generation Computers: Transistors (1956-1963): PDP-8, IBM1400 series, IBM 7090 and 7094, UNIVAC 1107, CDC 3600
- Third Generation Computers: Integrated Circuits (1964-1971): IBM 360, IBM 370, PDP-11, NCR 395, B6500, UNIVAC 1108
- Fourth Generation Computers: Micro-processors, VLSI (1971-1989): IBM PC, STAR 1000, APPLE II, Apple Macintosh, Alter 8800
- Fifth Generation Computers, ULSI, AI, Parallel processing

Scale of Integration

- Small Scale Integration (SSI), 1959 by Jack Kilby – logical gates: less than 100 transistors
- Medium Scale Integration (MSI), 1966 – multiplexor: 100-1000 transistors
- Large Scale Integration (LSI), 1970 - controller: 1000-10000 transistors
- Very Large Scale Integration (VLSI), 1980 – microprocessor: 10K-100K transistors
- Ultra Large Scale Integration (ULSI), 1990 – processor: 100K-10M transistors, up to 100nm
- Super Large Scale Integration (SLSI), 2000: >10M transistors



VLSI Circuit

Range of computer application

- Embedded control
- Real-time control
- Personal
- General purpose
- Mainframe
- High-performance
- Supercomputers

Supercomputers: top500.org

TOP500 List - November 2022 | T x +

top500.org/lists/top500/list/2022/11/

Home » Lists » Top500 » November 2022 » List

TOP500 LIST - NOVEMBER 2022

R_{max} and R_{peak} values are in PFlop/s. For more details about other fields, check the TOP500 description.

R_{peak} values are calculated using the advertised clock rate of the CPU. For the efficiency of the systems you should take into account the Turbo CPU clock rate where it applies.

←

1-100

101-200

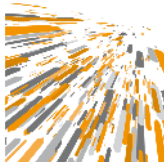
201-300

301-400

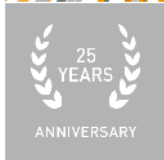
401-500

→


Rank	System	Cores	Rmax (PFlop/s)	Rpeak (PFlop/s)	Power (kW)
1	Frontier - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, HPE DOE/SC/Oak Ridge National Laboratory United States	8,730,112	1,102.00	1,685.65	21,100
2	Supercomputer Fugaku - Supercomputer Fugaku, A64FX 48C 2.2GHz, Tofu interconnect D, Fujitsu RIKEN Center for Computational Science Japan	7,630,848	442.01	537.21	29,899
3	LUMI - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, HPE EuroHPC/CSC	2,220,288	309.10	428.70	6,016



TOP500 LIST




25 YEARS ANNIVERSARY



NEWSLETTER SIGN UP

Activate Windows
Go to Settings to activate Windows.

Type here to search

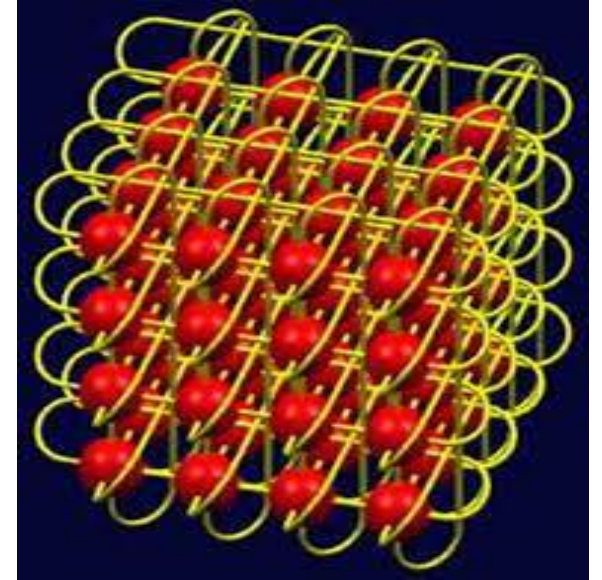


Coastal event

3:05 PM 2/26/2023

Supercomputers and clouds

IBM Blue Gene

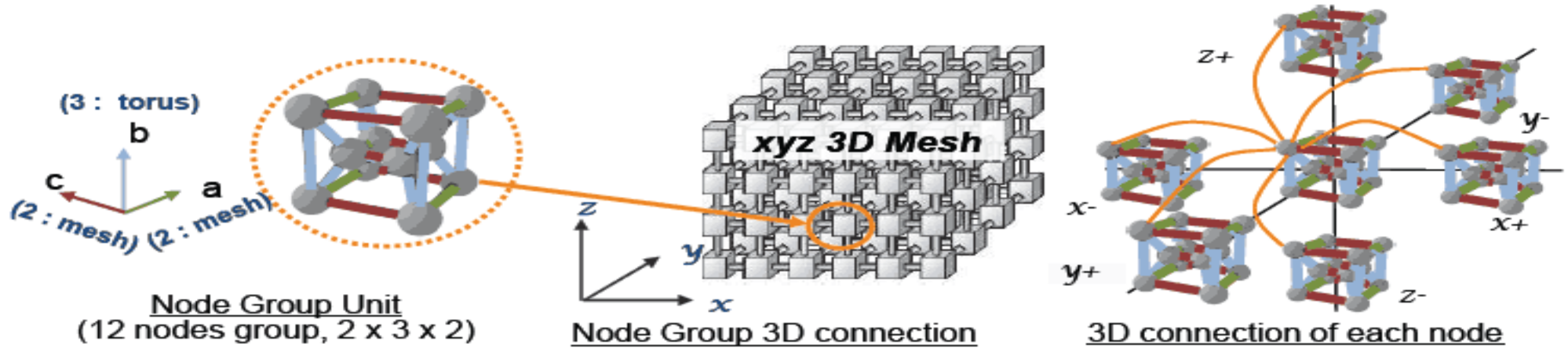


Blue Gene system with 65,000 nodes, are interconnected as a 64 x 32 x 32 three-dimensional torus. IBM Blue Gene/Q: 5D torus.

Supercomputer Fugaku

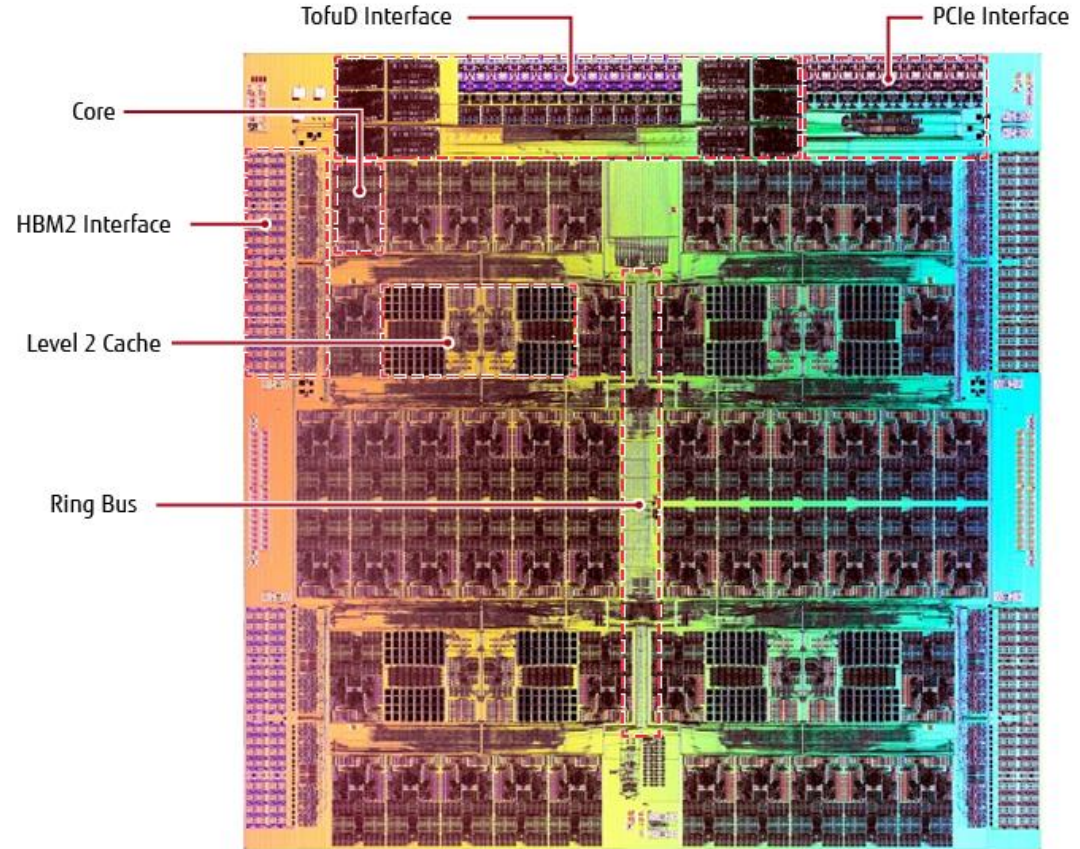


Tofu: Fujitsu's original 6D mesh/torus interconnect

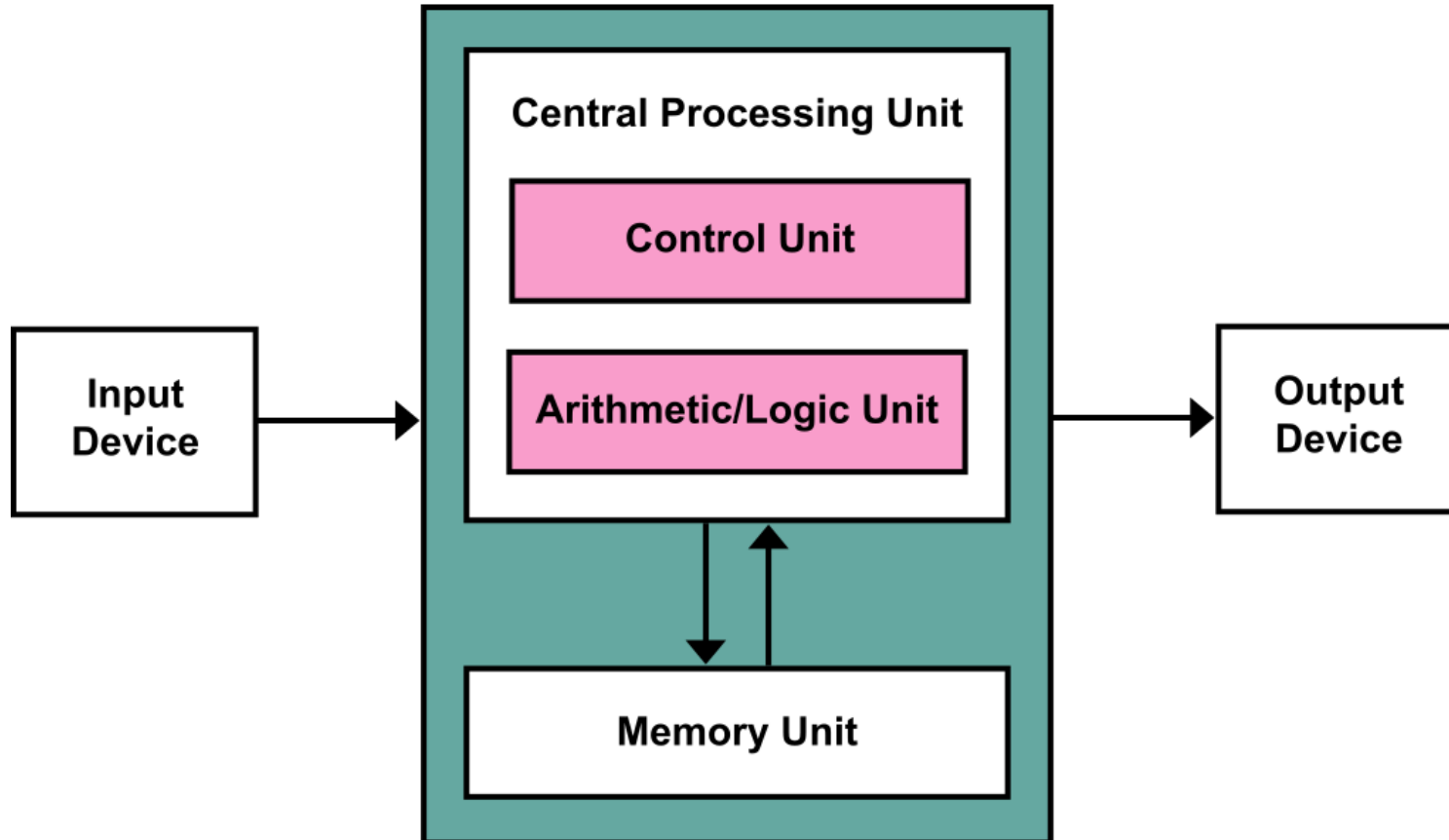


Tofu has a six-dimensional [mesh/torus topology](#), a scalability of over 100,000 nodes, and [full-duplex](#) links that have a peak bandwidth of 10 GB/s (5 GB/s per direction)

Processor Fujitsu AF64FX



Von Neumann computer architecture



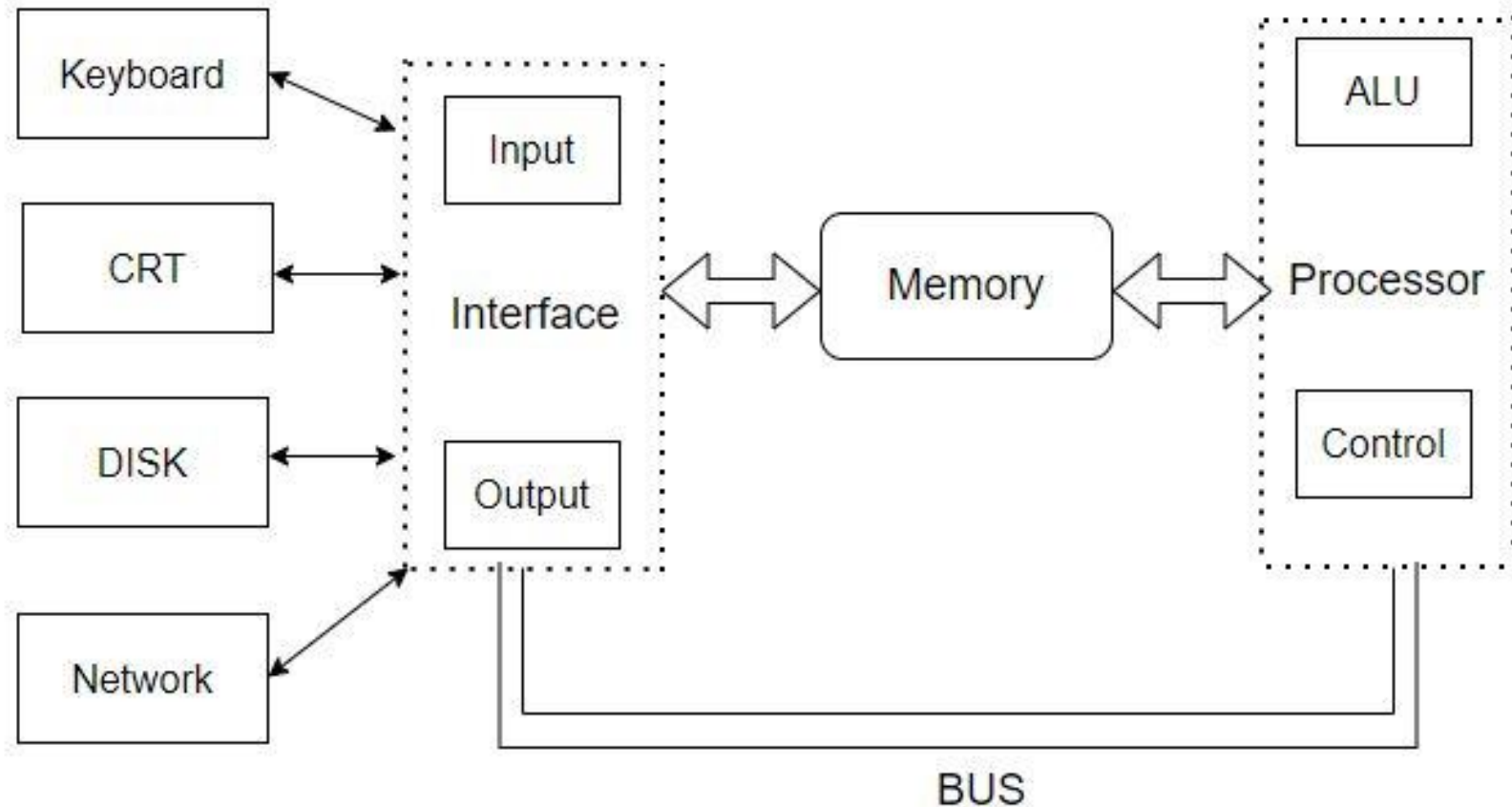
First Draft of a Report on the EDVAC, 1945

- A processing unit with both an arithmetic logic unit and processor registers
- A control unit that includes an instruction register and a program counter
- Memory that stores data and instructions
- External mass storage
- Input and output mechanisms

Von Neumann principles

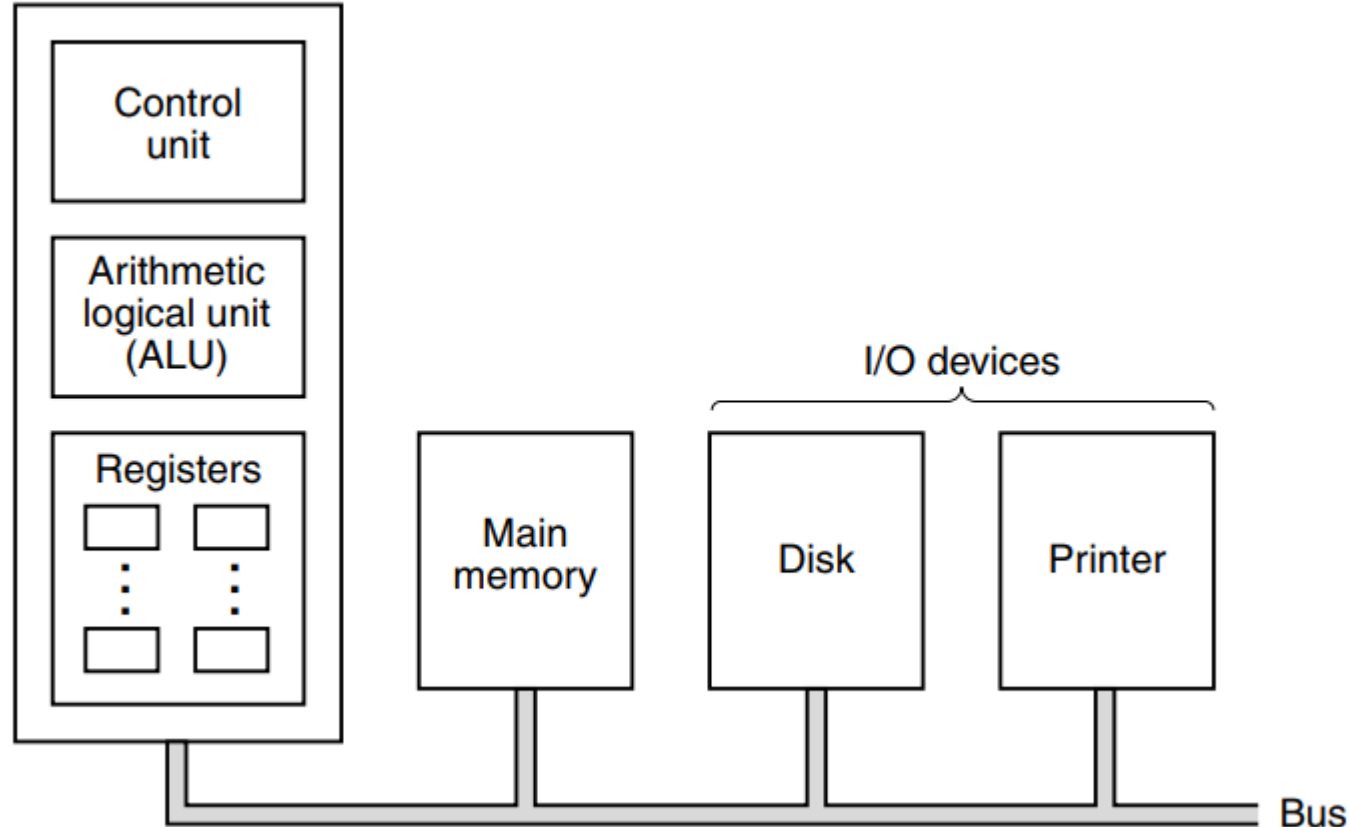
- Using binary numbering system
- Program control
- Memory stores program (instructions) and data
- Memory cells (words) are enumerated and accesses by their addresses (numbers)
- Conditional branching instruction

General scheme of computer

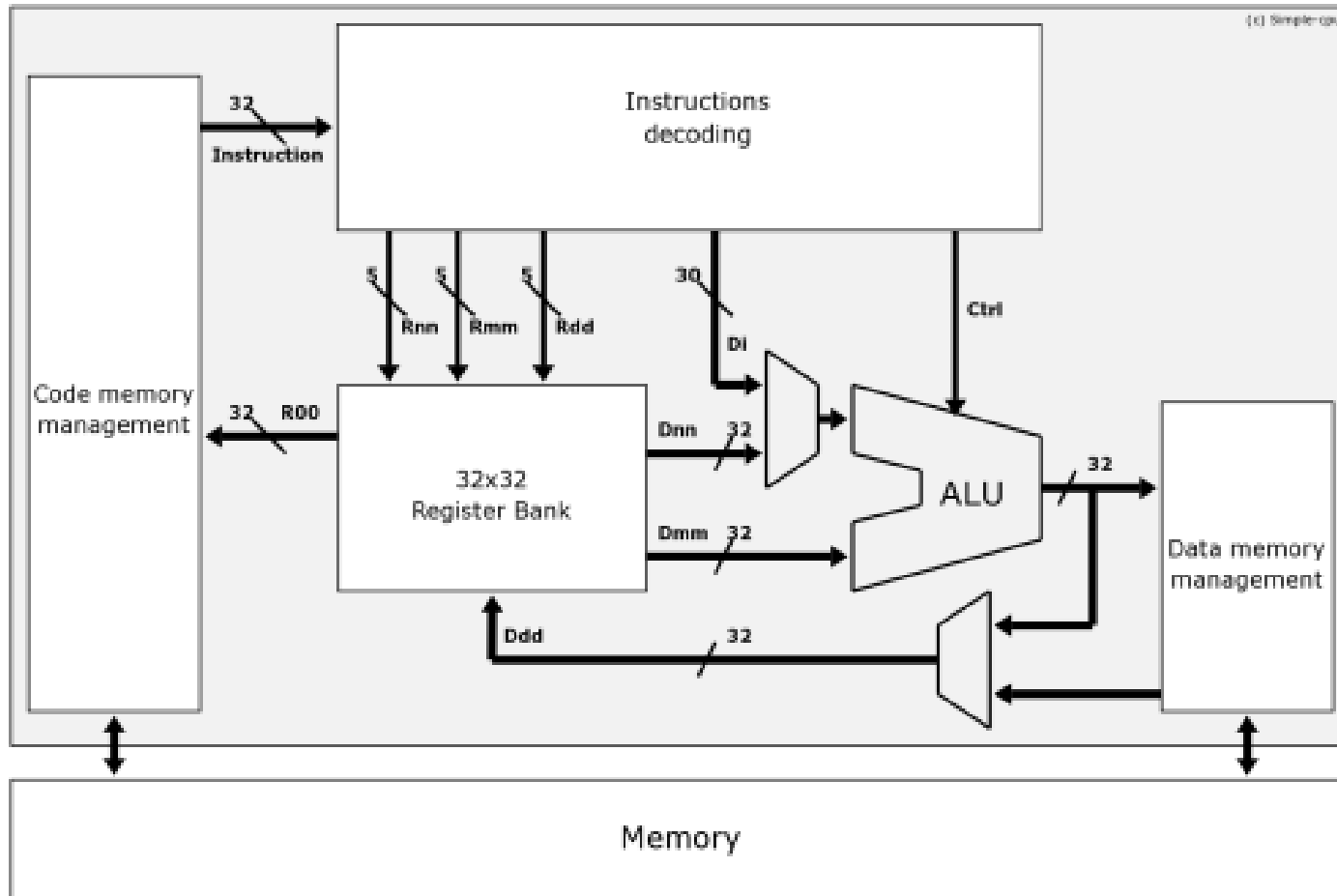


Common bus architecture

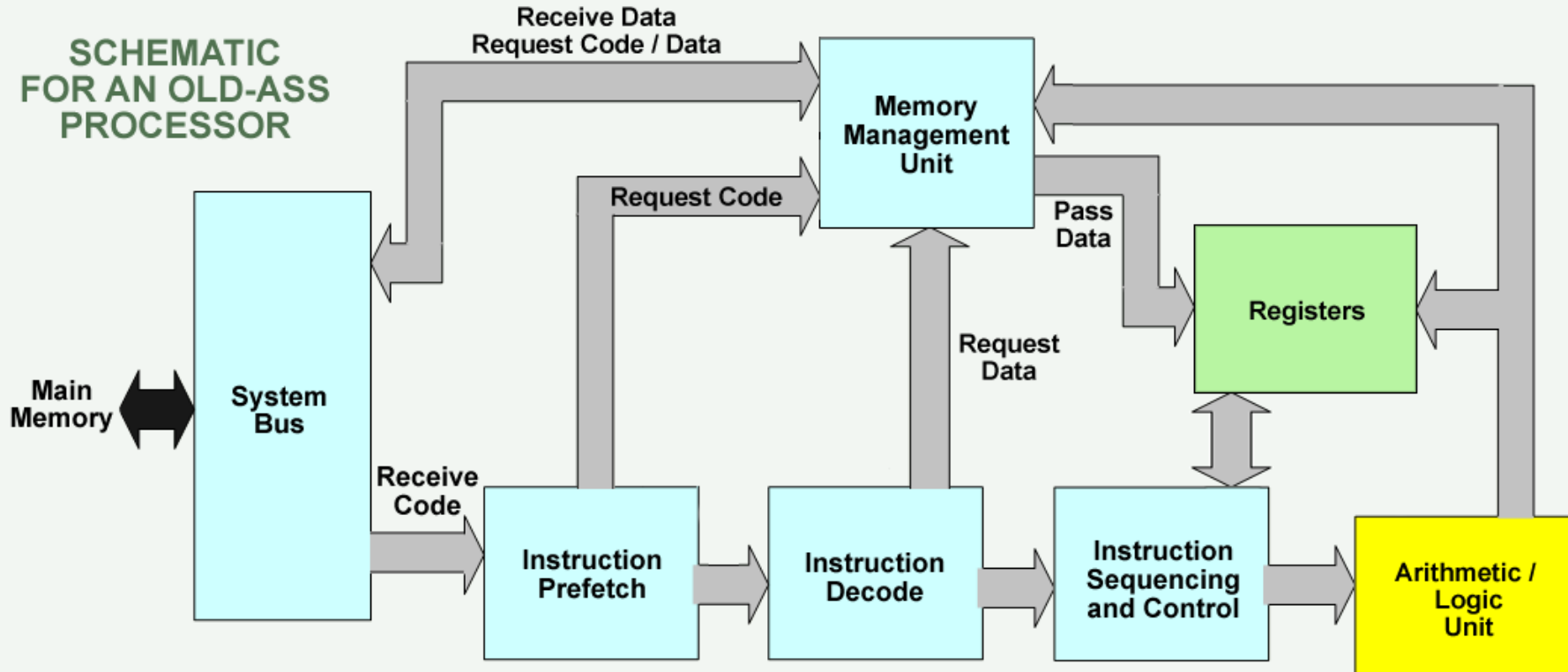
Central processing unit (CPU)



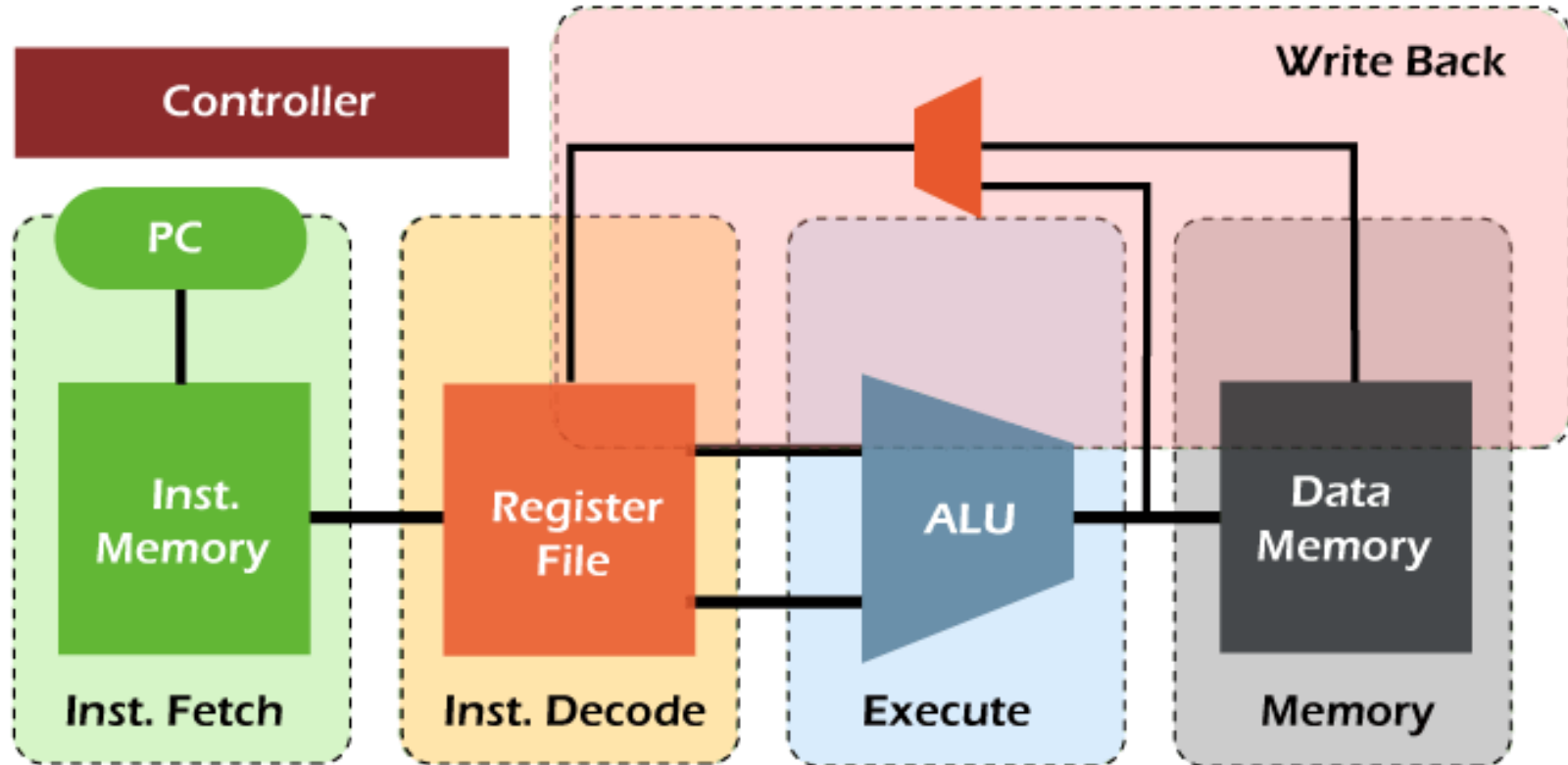
Processor scheme



Processor functioning



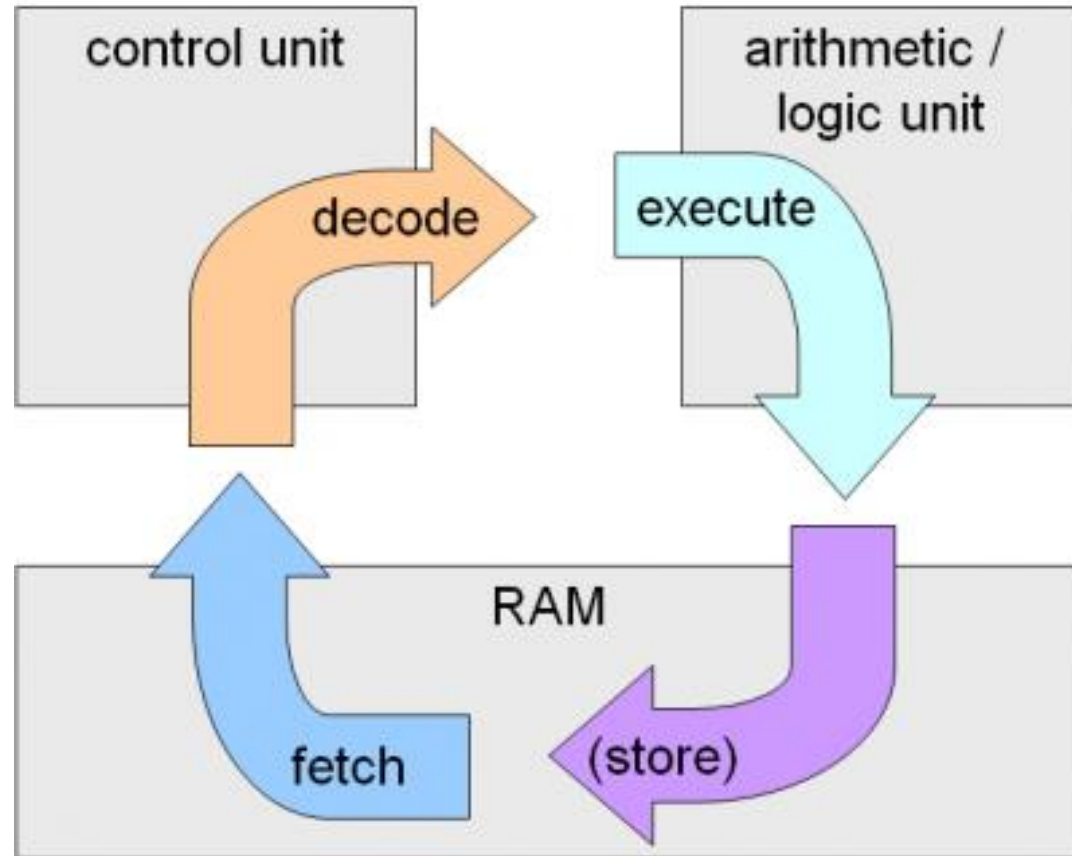
Processor pipeline



Processor instructions set

- data transfer (copy) operations,
- arithmetic operations,
- logical operations,
- branching operations,
- subroutine call-return,
- machine-control operations

Processor working cycle scheme



Processor working cycle description

- Use Program Counter (PC) to load (fetch) instruction from memory into dedicated current instruction register of processor
- Decode instruction
- Load (fetch) operands into input registers of ALU
- Start ALU to implement the operation
- Store result from ALU output register
- Increment PC by the instruction length: $PC = PC + dl$

Theoretical tree-addresses instruction format

Operation code	Address of operand 1	Address of operand 2	Address of result
-------------------	-------------------------	-------------------------	----------------------

(addr operand 1) <operation> (addr operand 2) -> (addr res)

Real formats of processor instructions

Operation code	Address of operand 1	Address of operand 2
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(addr op 1) <operation> (addr op 2) -> (addr op 1)

Operation code	Address of operand 2
----------------	----------------------

<accumulator> <operation> (addr operand 2) -> <accumulator>

Operation code

<operation> <accumulator> -> <accumulator>

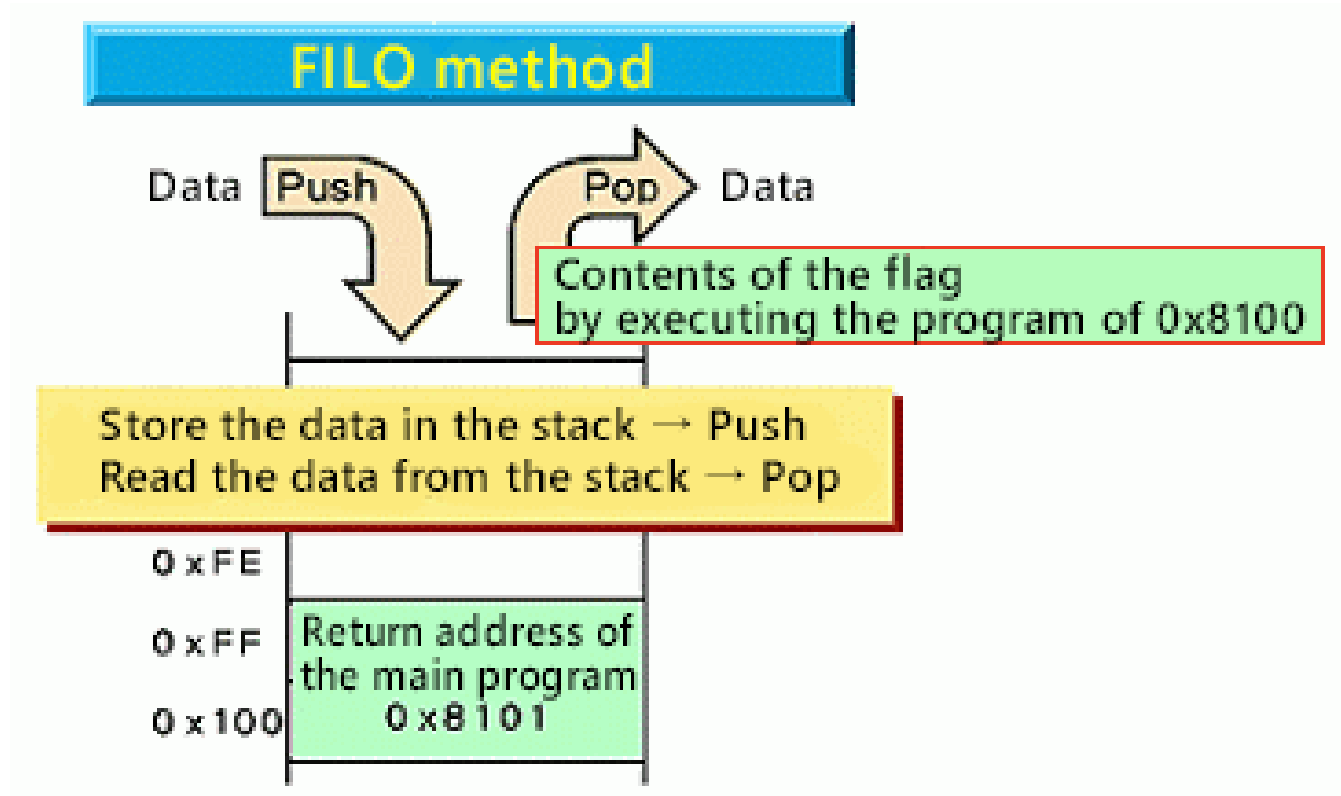
Addressing mode

- no address – implied operand – accumulator
- register – number (name) of processor register
- memory direct – content of memory word specified by address inside instruction
- immediate – operand inside instruction
- memory indirect - content of memory word specified by register(s) content
- variants:
 - based – base register plus offset (inside instruction),
 - indexed – base register plus index register plus offset (inside instruction)

Processor stack

- Last In First Out (LIFO) discipline
- Special register Stack Pointer (SP)
- Stack is implemented in memory, its top addressed by SP
- Two operations: Push and Pop
- subroutine call stores return address in stack
- interrupt procedure stores PSW in stack
- programming languages machines store in stack actual call parameters and local variables of functions

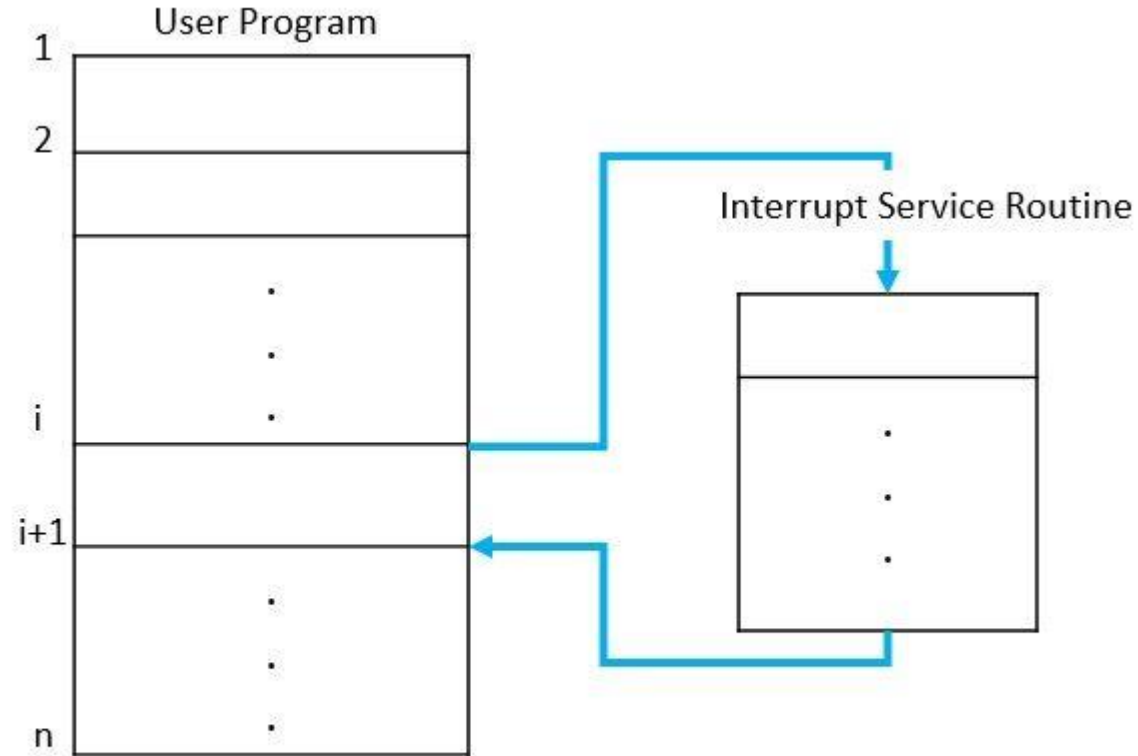
Processor stack scheme



Communication with input/output devices

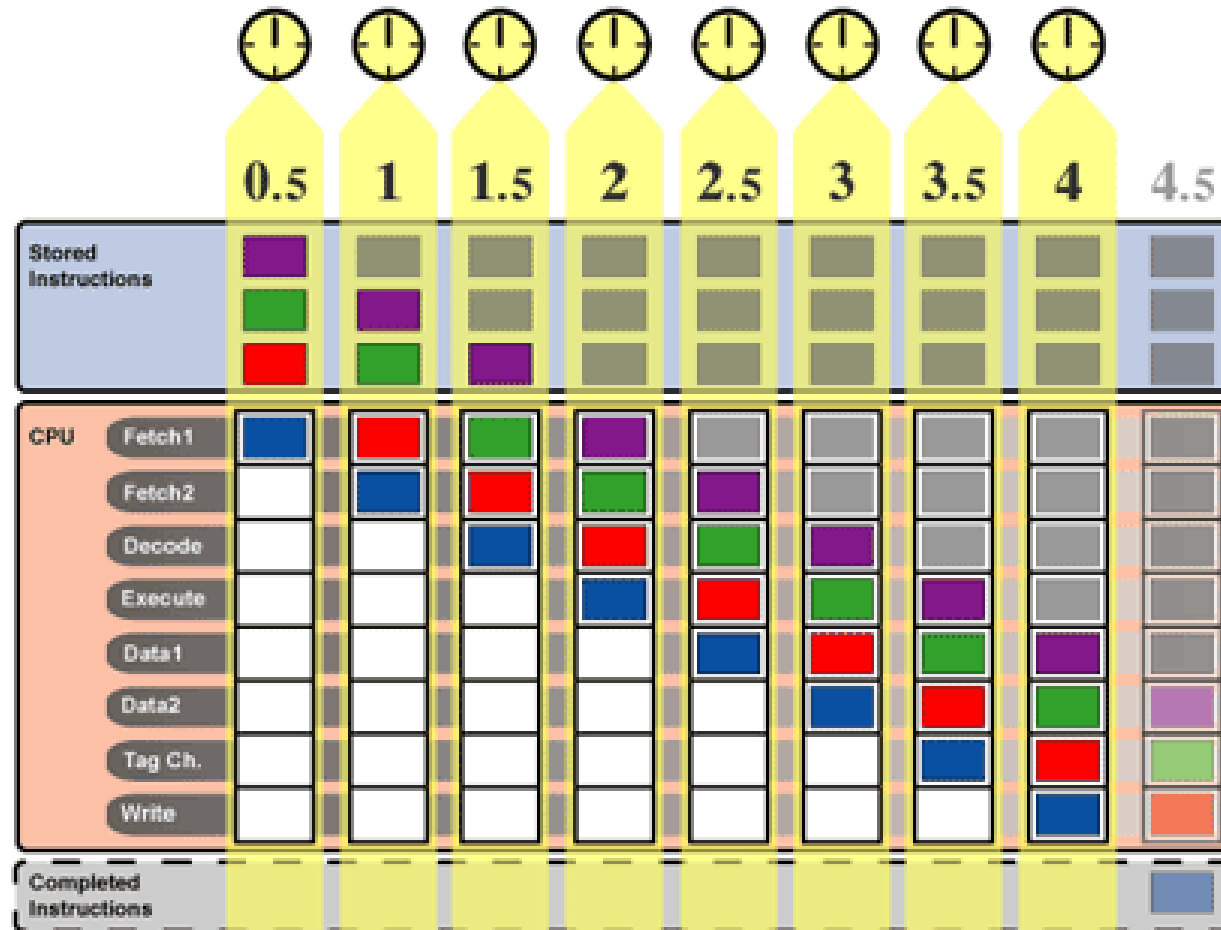
- input/output ports – special registers and special instructions – in/out to write into port and read port content; writing into ports starts actual functioning of external devices; reading from ports gives information on devices state and input data
- interrupt procedure – stop basic cycle, store PC and PSW into stack, load from the interrupt vector new PC and PSW; an interrupt resembles a subroutine call accompanied by PSW change

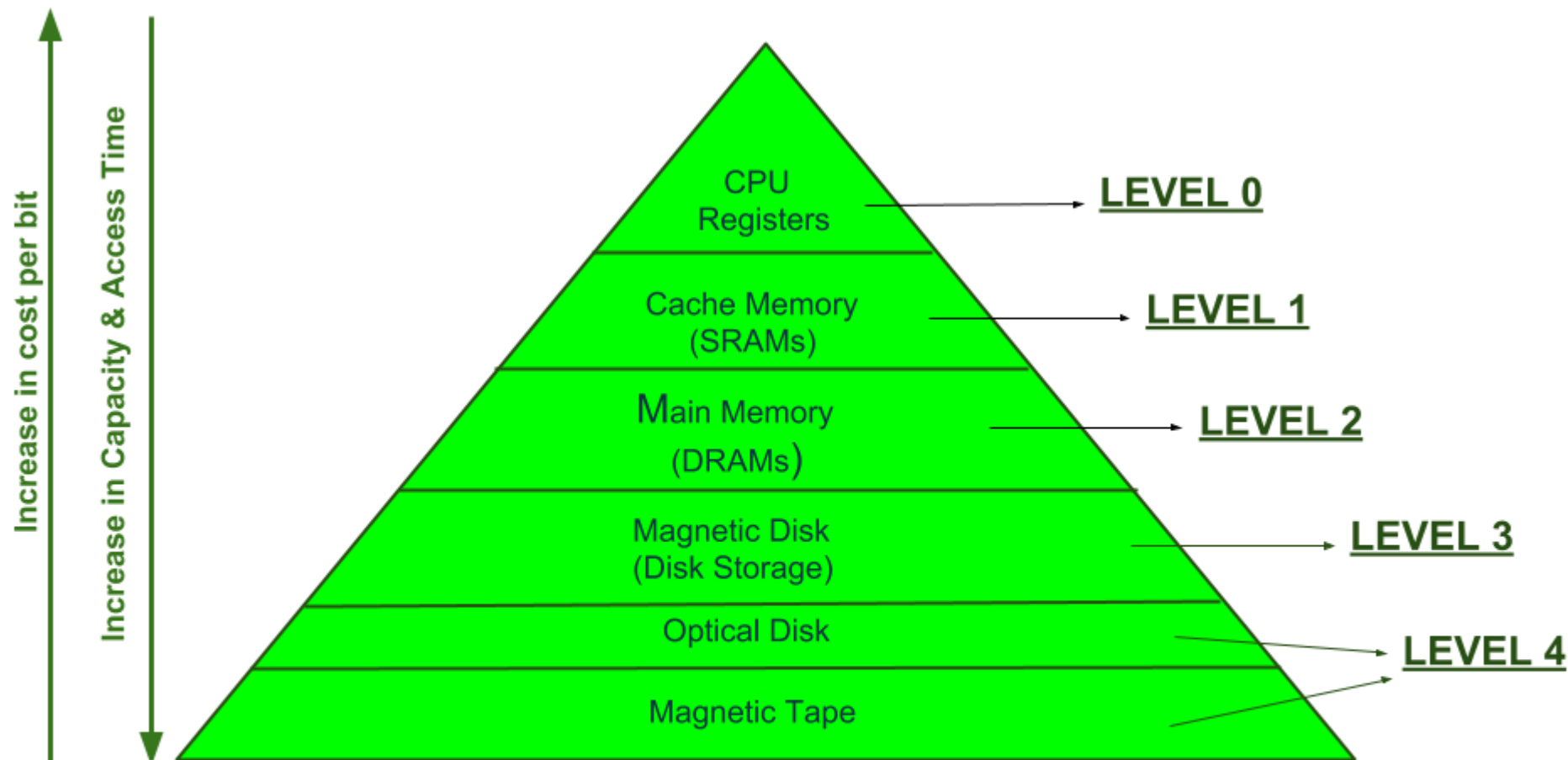
Interrupt scheme



Transfer Control Via Interrupts

Pipeline processing speed-up





MEMORY HIERARCHY DESIGN